Integrated Quadrupler Circuit in Coplanar Technology for 60 GHz Wireless Applications

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***Abstract*—This paper describes the design, the simulation and the measured results of a frequency quadrupler (x4 multiplier) circuit for mm-wave applications. The coplanar circuit was designed in a balanced configuration which makes it extremely small in area while maintaining excellent performance. A large number of circuits from several wafers were measured. The conversion loss is 4 dB and the harmonic suppression >20 dB with 6 dBm input power.**

I. INTRODUCTION

As data rates constantly increase, required bandwi(hs become larger and larger. This is especially a problem ior wireless systems because the allocated spectrum does not allow very high bandwidths. Therefore, the FCC opened a new unlicensed band from 59 (57) GHz to 64 GHz with very few restrictions. This band is very attractive for communication systems because there are no license fees and because of the unprecedented data rates possible. Wireless LAN, point-to-point links and backup links for fiber connections are some of the expected applications. All these systems require mm-wave sources for the up- and down-conversion. There are two main approaches: 1) a mm-wave fundamental oscillator or 2) a low frequency oscillator that is multiplied. The disadvantages of the fundamental oscillator are higher phase noise as well as difficulty in locking it to a reference oscillator. A divider circuit is required which is difficult to achieve for millimeter-wave frequencies. At 15 GHz in contrast, commercial prescalers are available (for example Agilent HMMC-300X) and locking is possible with all commercial parts. Therefore, a multiplied source is superior economically and in phase noise.

For 60 GHz applications, a circuit that quadruples the frequency is the ideal choice because locked 15 GHz oscillators with good phase noise are available. Compared to previous work [1]-[4], this design uses a very small chip area due to a new design methodology. The required input power is low and the circuit covers a bandwidth of 5 GHz.

II. CIRCUIT DESIGN

The devices used for the quadrupler circuits are Indium Phosphide High Electron Mobility Transistors (InP HEMTs) with a gate length of 0.1 micrometer and a transit frequency of 135-150 GHz. Coplanar technology was chosen because of the smaller ground inductance, the reduction of process steps, and the more efficient use of the chip area.

The design specifications for the quadrupler are given in Table I. Size was a very important factor because the circuit was to be dropped into an existing larger downconverter circuit. The challenge was to fit the whole quadrupler into a 0.8 mm^2 area.

Parameter	Specification
Input frequency	14.75-16 GHz
Output frequency	59-64 GHz
Output power	> 0 dBm
Chip size	1030 x 770 μm^2
Input power	<= 6 dBm

Table I: Specifications for the integrated quadrupler.

In a conventional circuit, quarterwave stubs are used in the matching networks and for filtering of the unwanted harmonics. These stubs are approximately 2 mm long at 15 GHz and could not be fit in the required chip size. To avoid these stubs, a balanced approach with a resistive input match was chosen.
Fig. 1 shows the block diagram of the quadrupler circuit.

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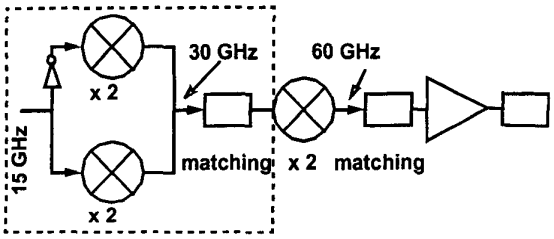


Fig. 1. Block diagram of the multiplier circuit. The dashed box contains the balanced 15 to 30 GHz doubler.

It consists of a balanced doubler (15 GHz to 30 GHz), a single-ended doubler (30 GHz to 60 GHz), and output amplifier with a filter. The filtering is integrated into the matching networks.

The balanced doubler consists of two Field Effect Transistors (FETs) which have the drains connected together. A small inverter FET changes the input signal phase of one of the FETs by 180 degrees. This topology sums the drain currents of the doubler FETs and therefore, cancels the fundamental frequency (and odd harmonics) and adds the second harmonic (30 GHz, and even harmonics). The FETs are biased near pinch-off where the efficiency is optimal for the doubling operation [5]. The voltage waveforms at the input of the FETs are shown in Fig. 2. The DC offset of –0.4 V corresponds to the pinch-off voltage. Ideally, the curves would have the same shape with a 180 degree phase shift. The difference in shape is due to the inverter FET which inverts one of the doubler input signals.

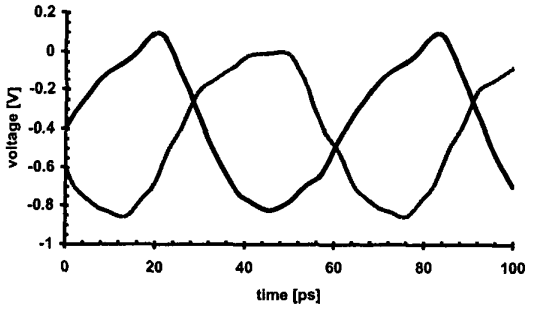


Fig. 2: Simulated voltage waveforms at the input of the doubler FETs (16 GHz).

The second doubler stage (30 to 60 GHz) is a conventional single ended doubler (Fig. 3) that has an open quarterwave stub to suppress the 30 GHz at the output. The transistor is biased near pinch-off also.

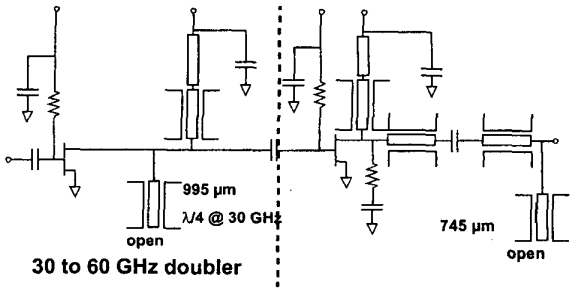


Fig. 3: Schematic of the second doubler stage and the output amplifier stage.

After the doubler, there is an amplifier stage with distributed matching acting as a filter for the undesired harmonics and providing matching for the 60 GHz signal. The open stub at the output suppresses the 3rd harmonic (45 GHz).

The chip photograph in Fig. 4 shows how compact the layout is. It was possible to meander the transmission lines in close proximity because compared to microstrip technology, coplanar technology reduces the coupling between lines.

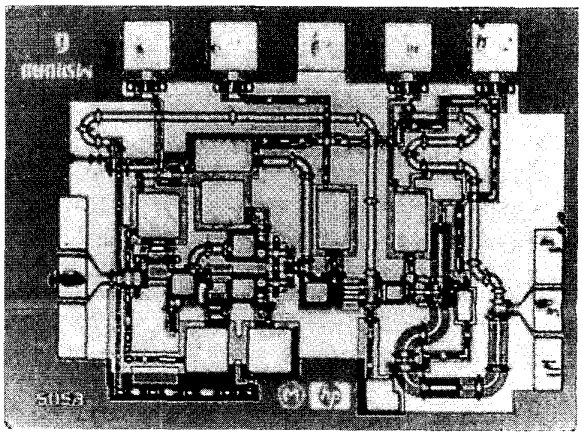


Fig. 4: Photograph of the quadrupler circuit. The chip area is only 0.8 mm^2.

III. MEASUREMENTS

On-wafer measurements were performed up to the 5th harmonic. An automated test set-up including software was developed (Fig. 5). The synthesizer (fundamental frequency) and spectrum analyzer were controlled by computer through an HPIB bus.

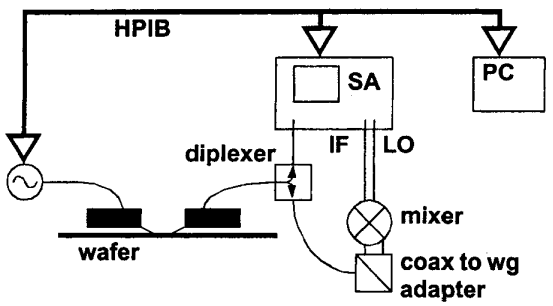


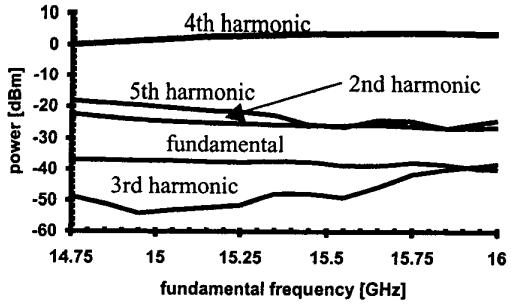
Fig. 5: Measurement set-up which allows the measurement of 5 harmonics. The computer sets the spectrum analyzer to internal mixer or external mixer depending on the harmonic being measured.

The software (HP-VEE program) sweeps the synthesizer from 14.75 GHz to 16 GHz and tunes the spectrum analyzer to the nth harmonic (n=1..5). Because the spectrum analyzer can only take input signals up to 50 GHz, a diplexer was used. One output of the diplexer was connected to the spectrum analyzer directly, the other to the unpreselected mixer. The computer changed the spectrum analyzer instrument state according to the harmonic to be measured (see Fig. 5). If the harmonic to be measured is higher than 50 GHz, the external mixer is used, otherwise the internal mixer is selected. This set-up can measure 5 harmonics without any hardware changes.

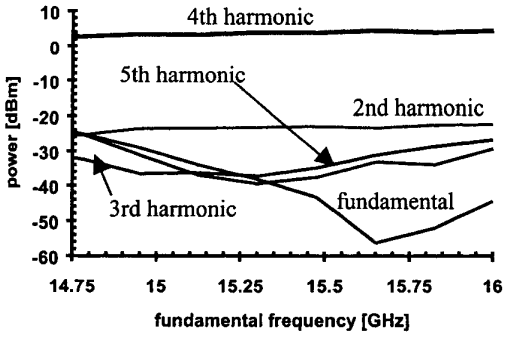
Fig. 6 compares a typical measurement and the simulation. The simulation was performed with a Root model [6], which is measurement based. This model takes into account many phenomena not captured in analytical models. It predicts the harmonics well for large input signals as long as the voltages and currents stay within the extracted range. Problems can arise when signals fall in between two measurement points where a spline interpolation is used.

Measurement agrees well with the simulation. It should be noted that while the agreement is good for even harmonics, it is only fair for the odd harmonics because the cancellation of the odd harmonics in the balanced doubler is very sensitive to any phase errors. In contrast, the even harmonics are not affected by slight phase errors to the same extent.

The DC power for this measurement was 90 mW with a supply voltage of 1.5 V.



a) Simulation



b) Measurement

Fig. 6: The output power of the five harmonics is shown as a function of the fundamental frequency. The suppression of the harmonics is better than 20 dB.

1550 circuits from 5 different wafers were measured. A circuit yield up to 58% was achieved.

IV. Conclusions

A fully integrated quadrupler circuit has been shown. The circuit described herein can be used in a local oscillator chain or in a transmit chain of unlicensed 60 GHz wireless applications. The circuit is exceptionally small because the first doubler stage was designed utilizing a balanced configuration and because coplanar transmission lines can be positioned closely without significant coupling.

This quadrupler's excellent performance simplifies a wireless system considerably because there is no need for additional amplifiers to increase the power levels. For example, the quadrupler can drive a passive FET mixer directly. The advantages are twofold:

- Since there are fewer components, assembly is simplified, test time is decreased, and yield is

increased.

- The system performance is improved because bondwire connections are eliminated.

The quadrupler circuit helps to reduce costs because the VCO at 15 GHz (instead of 60 GHz) can be locked with commercial parts. Taking into account these benefits, this quadrupler helps the to make 60 GHz wireless systems commercially viable.

ACKNOWLEDGMENT

I would like to thank Rory Van Tuyl for his support and encouragement of this work.

The models were extracted by David Root's group. Special thanks go to Dan Scherrer.

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